WHAT IS CLAIMED IS:

1. A circuit for providing write pre-compensation utilizing read signal timing, comprising:

a first phase clock source for generating a first clock signal having a first phase and being synchronized with a read signal of the read path;

a second phase clock source for generating a second clock signal having a second phase at a predetermined phase difference with the first clock signal; and

a write pre-compensation circuit for using the first and second clock signals to shift write data to achieve write data comprising a first desired pre-compensation.

2. The circuit of claim 1, wherein the second phase clock source generates the second clock signal in response to a read phase select position signal from the read path and a write phase select position signal.

3. The circuit of claim 2, wherein the write pre-compensation circuit further comprises:

write logic for receiving write data;

a first and second latch, coupled to the write logic, the first and second latch receiving the write data from the write logic and using the first clock signal to supply a first data signal and using the second clock signal to supply a second data signal; and

a data selector, coupled to the write logic, for receiving a data select signal from the write logic and outputting the first or second data signal based on a state of the data select signal.

4. The circuit of claim 1, wherein the write pre-compensation circuit further comprises:

write logic for receiving write data;

a first and second latch, coupled to the write logic, the first and second latch receiving the write data from the write logic and using the first clock signal to supply a first data signal and using the second clock signal to supply a second data signal; and

a data selector, coupled to the write logic, for receiving a data select signal from the write logic and outputting the first or second data signal based on a state of the data select signal.

5. The circuit of claim 1 further comprising a coarse phase clock source, wherein the first and second phase clock sources are first and second fine phase clock sources, the first and second fine phase clock sources generating the first and second clock signals based on a coarse phase signal from the coarse phase clock source.

6. The circuit of claim 1, wherein the second phase clock source follows the phase of the first clock phase source during a read operation.

7. The circuit of claim 6, wherein the phase difference between the second phase clock source and the first phase clock source is maintained.

8. The circuit of claim 1, wherein the phase difference between the second phase clock source and the first phase clock source is maintained.

9. The circuit of claim 1, wherein the first and second phase are changed to provide write data comprising a second desired pre-compensation.

10. The circuit of claim 1 further comprising at least one additional phase clock source, the at least one additional phase clock source providing at least one additional pre-compensation state.

11. A magnetic storage device, comprising:

a magnetic storage medium for recording data thereon;

a motor for moving the magnetic storage medium;

a head for reading and writing data on the magnetic storage medium;

an actuator for positioning the head relative to the magnetic storage medium; and

a data channel for processing encoded signals on the magnetic storage medium, the data channel comprising a first phase clock source for generating a first clock signal having a first phase and being synchronized with a read signal of the read path, a second phase clock source for generating a second clock signal having a second phase at a predetermined phase difference with the first clock signal and a write pre-compensation circuit for using the first and second clock signals to shift write data to achieve write data comprising a first desired pre-compensation.

12. The magnetic storage device of claim 11, wherein the second phase clock source generates the second clock signal in response to a read phase select position signal from the read path and a write phase select position signal.

13. The magnetic storage device of claim 12, wherein the write pre-compensation circuit further comprises:

write logic for receiving write data;

a first and second latch, coupled to the write logic, the first and second latch receiving the write data from the write logic and using the first clock signal to supply a first data signal and using the second clock signal to supply a second data signal; and

a data selector, coupled to the write logic, for receiving a data select signal from the write logic and outputting the first or second data signal based on a state of the data select signal.

14. The magnetic storage device of claim 11, wherein the write pre-compensation circuit further comprises:

write logic for receiving write data;

a first and second latch, coupled to the write logic, the first and second latch receiving the write data from the write logic and using the first clock signal to supply a first data signal and using the second clock signal to supply a second data signal; and

a data selector, coupled to the write logic, for receiving a data select signal from the write logic and outputting the first or second data signal based on a state of the data select signal.

15. The magnetic storage device of claim 11 further comprising a coarse phase clock source, wherein the first and second phase clock sources are first and second fine phase clock sources, the first and second fine phase clock sources generating the first and second clock signals based on a coarse phase signal from the coarse phase clock source.

16. The magnetic storage device of claim 11, wherein the second phase clock source follows the phase of the first clock phase source during a read operation.

17. The magnetic storage device of claim 16, wherein the phase difference between the second phase clock source and the first phase clock source is maintained.

18. The magnetic storage device of claim 11, wherein the phase difference between the second phase clock source and the first phase clock source is maintained.

19. The magnetic storage device of claim 11, wherein the first and second phase are changed to provide write data comprising a second desired pre-compensation.

20. The magnetic storage device of claim 11 further comprising at least one additional phase clock source, the at least one additional phase clock source providing at least one additional pre-compensation state.

21. A method for providing write pre-compensation utilizing read signal timing, comprising:

generating a first phase clock signal having a first phase and being synchronized with a read signal of a read path;

generating a second phase clock signal having a second phase at a predetermined phase difference with the first clock signal; and

using the first and second clock signals to shift write data to achieve write data comprising a first desired pre-compensation.

22. The method of claim 21, wherein the generating the second clock signal is based on a read phase select position signal from the read path and a write phase select position signal.

23. The method of claim 22, wherein the using the first and second clock signals to shift write data to achieve write data comprising a first desired pre-compensation further comprises:

receiving write data;

providing the write data to a first latch and a second latch;

using the first clock signal to latch the first latch to supply a first data signal;

using the second clock signal to latch the second latch to supply a second data signal; and

outputting the first or second data signal based on a state of a received data select signal.

24. The method of claim 21, wherein the write pre-compensation circuit further comprises:

receiving write data;

providing the write data to a first latch and a second latch;

using the first clock signal to latch the first latch to supply a first data signal;

using the second clock signal to latch the second latch to supply a second data signal; and

outputting the first or second data signal based on a state of a received data select signal.

25. The method of claim 21, wherein the generating a first phase clock signal and generating a second phase clock signal further comprises:

generating a coarse phase clock signal;

generating the first and second phase clock signals based on the coarse phase clock signal.

26. The method of claim 21, wherein the generating a first phase clock signal and generating a second phase clock signal further comprises generating the second the second phase clock signal with a phase that follows the phase of the first clock phase signal during a read operation.

27. The method of claim 26, wherein the generating a first phase clock signal and generating a second phase clock signal further comprises maintaining the phase difference between the second phase clock signal and the first phase clock signal.

28. The method of claim 21, wherein the generating a first phase clock signal and generating a second phase clock signal further comprises maintaining the phase difference between the second phase clock signal and the first phase clock signal.

29. The method of claim 21, wherein the generating a first phase clock signal and generating a second phase clock signal further comprises changing the phase of the first and second phase clock signals to provide write data comprising a second desired pre-compensation.

30. The method of claim 21 further comprising generating at least one additional phase clock signal for providing at least one additional pre-compensation state.